Experiment 10
Digital Design
Pre-Lab Report

Half Adder

From the table in Figure 3 we obtained:

$$S_1 = \bar{A}_1 B_1 + A_1 \bar{B}_1$$
$$C_1 = A_1 B_1$$

In the laboratory session you will only be provided with a 74LS00 chip which is a quad two input NAND gate chip and a 74LS04 hex inverter chip. In order to be able to implement the design you need to convert the equations of S1 and C1 into an equivalent algebraic form that only uses NAND gates and inverters.
Use demorgan's theorem to prove that

$$S_1 = \overline{\overline{A(\overline{AB})} \cdot \overline{B(\overline{AB})}}$$

C = AB = (A'+B')'by Demorgan's theorem
S1=((AC')'(BC')')'=((A'+C)(B'+C))'=AC'+BC'
but C'=(A'+B')''=A'+B'
then, S1=A(A'+B')+B(A'+B')=AA'+AB'+BA'+BB'
AA'=0
BB'=0
then, S1=0+AB'+BA'+0
S1=AB'+BA